Compensated aspect ratio dependent etching (CARDE) using gray-scale technology

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Abstract

We report a photoresist offset method using gray-scale technology to counteract the effect of aspect ratio dependent etching (ARDE), achieving controlled etch depths across a range of aspect ratios. Previously, we have reported the first fabrication of a deep phase Fresnel lens (PFL) in silicon through the use of gray-scale technology. As each PFL ridge becomes thinner at larger radii of the PFL, ARDE causes a significant reduction in profile accuracy. Thus, in this paper, a compensated aspect ratio dependent etching (CARDE) process is proposed and demonstrated to enable controlled ridge heights/depths on large diameter PFLs containing a variety of ridge widths. A compensation function is used during optical mask design to incorporate a photoresist offset, defining wide ridges with higher gray levels to locally modulate the time of etching, effectively giving thin ridges a head start during the etch. Multiple PFL profiles, both compensated and uncompensated, are designed and fabricated. Using a phasor-based profile evaluation method, PFLs fabricated using the CARDE process are shown to exhibit an increase in profile accuracy and calculated lens efficiency.
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1. Introduction

Deep reactive ion etching (DRIE) [1] has become a standard fabrication technique in the area of micro-electro-mechanical systems (MEMS). Since DRIE is a time-multiplexed derivative of traditional reactive ion etching (RIE), it often exhibits some of the same etching characteristics traditionally seen during RIE of silicon. One of the most common phenomenon seen in these dry plasma processes is RIE-lag, where smaller features etch at a slower rate than larger features.

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This effect, also referred to as aspect ratio dependent etching (ARDE), has been observed and/or modeled in RIE and DRIE by numerous groups [2–4].

The physical processes behind ARDE are quite complicated. However, qualitatively, ARDE can be attributed to the changes in transport properties of ions, etchants and sidewall inhibitors depending on feature size. This size dependence causes a corresponding difference in the etch rate of each feature. Thus, in RIE, small trench features typically etch slower than large trench features, exhibiting a 'lag' behind the etch depths of the larger features. Additional mechanisms have been proposed that may contribute to ARDE specifically in time-multiplexed systems, such as the insufficient removal of the bottom passivation layer due to the reduction in the angular and energy distribution of ion and neutral flux at increased aspect ratios [3,5]. Suggestions have also been made to reduce the ARDE effect by using lower coil power to reduce the etch rate's dependence on the ion energy [6]. Other approaches have been demonstrated to achieve consistent etch depths across different aspect ratios by using additional processing methods, such as a combination of dry etching followed by wet anisotropic etching [7], but this adds an undesirable process step.

While a universal solution to the problem of ARDE is unlikely, solutions that can be easily adapted to a variety of structures and other process requirements are most desirable. For deep etches using DRIE, the lag exhibited by smaller features may reach the 10's of micrometers due to different etch rates and a constant etching time for the entire pattern. However, if the etch time of each feature could be modulated depending on the feature size, the etch rate of each feature size could remain different, and a consistent etch depth would be achieved. In a sense, smaller features with lower etch rates would be afforded extra etch time to achieve the desired overall etch depth, effectively getting a 'head-start' to offset the difference in etch rate. With a planar mask, such a proposal is unrealistic, but with the advancement of gray-scale technology, differential height masking layers may be created to achieve such behavior in a single lithography and etching step.

In this paper, we outline a method by which a photoresist offset may be incorporated into 3D gray-scale structure designs to counteract the effects of aspect ratio dependent etching exhibited during the transfer of the photoresist pattern into the silicon substrate. This compensated aspect ratio dependent etching (CARDE) process is then used in the development of a silicon X-ray phase Fresnel lens (PFL) to increase the profile accuracy across a range of feature sizes. A phasor-based profile evaluation method is introduced to evaluate the fabricated silicon PFL profiles. PFLs fabricated using the CARDE process are shown to exhibit an increase in profile accuracy and calculated PFL efficiency when compared to uncompensated designs. Finally, limitations of this new process are discussed.

2. Gray-scale technology and CARDE

Gray-scale lithography is a method of creating arbitrary 3D shapes in photoresist. Sub-resolution pixels and pitches locally modulate the intensity seen by a positive photoresist film, exposing each location to a specified depth [8,9]. After a controlled development step, a 3D photoresist profile remains and is used as a masking layer during dry-anisotropic etching to transfer this pattern into the underlying substrate [10,11]. During the etch process, more silicon becomes exposed as the photoresist is removed. Thus, the relative etch rate of silicon to photoresist (referred to as 'etch selectivity') determines the amplification of the vertical dimensions in photoresist into the vertical dimensions in silicon. Since the photoresist masking layer is slowly removed during the etch, the time that the silicon is exposed to the plasma is inversely proportional to the local thickness of the photoresist masking layer. By incorporating an offset in the design of the gray-scale photoresist masking layer, the etching time of each feature size can be tailored appropriately, creating a compensated aspect ratio dependent etching (CARDE) process. Depending on the desired total etch depth, the 'head start' required by smaller features will change, altering the amount of offset required in the photoresist design. Such a process could be

extremely advantageous because only a single lithography and dry-etching step are required, and no additional pre- or post-processing steps are necessary. Although tight process controls are required during the two main process steps, the CARDE process can be easily integrated into a wide range of structures and applications, becoming an enabling technology in the MEMS community.

The application of the CARDE process presented here is in the development of a silicon phase Fresnel lens (PFL). Such a lens could serve as a low energy test bed for a next generation astronomical imaging system with the potential to provide unprecedented angular resolution and sensitivity for measurements of high energy astrophysical phenomena [12,13]. Recently, we demonstrated that gray-scale technology could be used to fabricate silicon PFLs with stepped profiles, using many 'gray levels', enabling more than double the maximum theoretical efficiency of a binary profile [14]. An ideal PFL profile is shown in Fig. 1, along with an example 4-level stepped profile approximation. A Gaussian approximation method was used to distribute the sub-resolution pixels during optical mask design to emulate the complicated PFL profile. Precise etch selectivity control during DRIE was accomplished by incorporating an oxygen-only step to the standard Bosch DRIE cycle to achieve the low etch selectivity necessary to 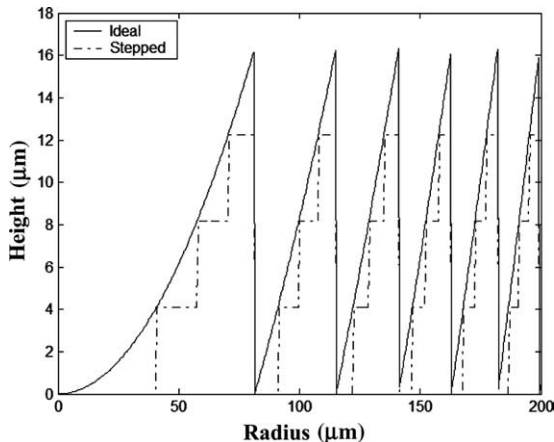transfer the photoresist pattern to the specified depth in the silicon. However, since a PFL profile is composed of many angled ridges that decrease in width at increasing radii, it was observed that the etch depth of each PFL ridge decreased at large radii. This ARDE resulted in progressively worse profile accuracy at the PFL extremes.

3. CARDE PFL design

The profile accuracy of the outer PFL ridges becomes very important because the annular ring created by each PFL ridge will comprise an equal area. Thus, a single thin ridge at a large radius carries as much weight as a central wide ridge. As the radius of the PFL is increased, many thin ridges are added and begin to dominate the overall PFL performance. Therefore, design and fabrication considerations should focus on maximizing the outer ridge efficiency. Due to the slower etch rate of thin ridges compared to wide ridges, a standard etch time cannot simultaneously achieve appropriate etch depths at both extremes. However, if the wide central ridges could be designed to start etching after a short delay, their faster etch rate would cause them to 'catch-up' to the thin outer ridges later in the etch, achieving a consistent etch depth.

Currently, a 80-m long X-ray beam line is being brought on-line at the NASA-Goddard Space Flight Center, which will provide easy access for testing and characterization of silicon PFLs. The ideal PFL profile for this setup is [14],

$$t(r) = mt_{2\pi}\text{MOD}\left[\left(\frac{r}{A\sqrt{m}}\right)^2, 1\right], \tag{1}$$

where r is the radius, $t_{2\pi}$ is the thickness of silicon required to produce a 2π phase shift, m is the number of 2π phase depths, and A is a function of the desired focal length (f) and photon energy (E),

$$A = 49.8\sqrt{\frac{f \text{ (m)}}{E \text{ (keV)}}} \ \mu\text{m}. \tag{2}$$

For this setup, the desired focal length is 17.1 m and the available iron target can provide $\sim$6.4 keV photons, which together yield a value of 81.4 μm for A and 16.3 μm for $t_{2\pi}$ [15].

Fig. 1. An example ideal PFL profile and a 4-level stepped profile approximation.

An investigation of (1) and (2) reveals that as the radius is increased, each ridge becomes thinner and has a higher aspect ratio (for any given photon energy). To collect an appreciable amount of flux from the X-ray source, PFLs with a minimum of 1 mm diameter are desired. Additionally, a 4π phase depth design will be used, effectively doubling the width of each ridge in photoresist and doubling the height in silicon (the aspect ratios do not change). The ridge width at a radius of 500 μm for a 4π phase depth design is calculated to be $\sim$13 μm, and the ideal ridge height will be 32.6 μm ($2t_{2\pi}$).

Ridge widths $\sim$13 μm wide will cause appreciable ARDE compared to the wide central ridges ($>$100 μm), reducing the overall profile accuracy and efficiency of the lens. Since these different etch depths are essentially caused by a constant etch time and different etch rates, to achieve a constant etch depth for all feature sizes, we could attempt to adjust some of the many etch process parameters. Unfortunately, any resulting process will likely come at the cost of limited control over etch selectivity and other characteristics. Instead, we choose to modulate the etch time of each feature to counteract the differences in etch rates, which should leave significant flexibility for subsequent tuning of other etch characteristics.

For this demonstration, a set of 16 gray levels, each corresponding to a particular pixel size on the mask, was distributed throughout each PFL design to define the photoresist height at each location on the lens. The PFL radius was designed to be 501 μm to contain 19 full ridges with a minimum ridge width of 13 μm. The conventional, or uncompensated, profile is included as a reference point and is thus a modified version of (1),

$$t(r) = PR_{\max}\mathrm{MOD}\left[\left(\frac{r}{81.4\sqrt{2}}\right)^2, 1\right], \qquad (3)$$

which normalizes the periodic modulus function to the maximum photoresist height ($PR_{\max}$) available in the design (remembering that etch selectivity during DRIE will determine the final vertical dimensions in silicon).

For the CARDE PFL, a compensating function ($\delta(r)$) is introduced to the above method. Since the

widths of the PFL ridges steadily decrease as the radius increases, a linearly decreasing compensation function was used for simplicity,

$$\delta(r) = -\left(\frac{\delta_0}{R_{\max}}\right)r + \delta_0, \qquad (4)$$

where $R_{\max}$ is the radius at which no compensation will be used and δ_0 is the maximum normalized offset in the center of the PFL. The compensation function is then incorporated into the thickness profile of (3),

$$t(r) = \left\{(PR_{\max} - \delta(r))\mathrm{MOD}\left[\left(\frac{r}{81.4\sqrt{2}}\right)^2, 1\right]\right\} + \delta(r). \qquad (5)$$

An example compensated ideal profile, with $\delta_0 = 0.10$ and $R_{\max} = 500$ μm, is shown in Fig. 2. The wide ridges at the center of the lens that will etch quickly in silicon, are now defined using higher gray levels (i.e., thicker photoresist). Thus, the central wide ridges will begin etching after a delay, while the thin outer ridges will begin transferring into the silicon immediately, effectively getting a head start. At a certain point later in the etch, the wide central ridges will catch up to the thin outer ridges and a consistent etch depth/ridge height will be achieved. Since the outer PFL ridges will dominate the performance of the overall PFL
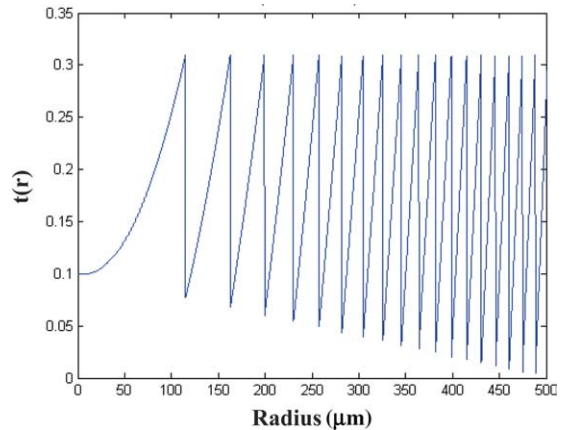

Fig. 2. A compensated photoresist PFL profile.

(as explained earlier), the appropriate etch time for our devices will be determined by the full transfer of the outer ridges.

Although a linearly decreasing compensation function is used here for a PFL, the same integration methodology can be adopted to virtually any desired 3D profile with varying feature widths by simply adjusting the compensation function to an appropriate form (such as piecewise constant design for large plateaus).

4. Profile evaluation method

Due to the cost of testing PFLs in an X-ray beam line, it would be advantageous to develop a method for predicting the approximate expected efficiency of various PFL profiles from their fabricated geometries. The evaluation method developed below is based on the ray tracing diagram shown in Fig. 3, and will serve as a quantitative evaluation of the accuracy of our gray-scale fabrication techniques.

Assumptions are made about the system to isolate the effect of the fabricated lens profile accuracy on the efficiency. First, it is assumed that an ideal photon source is used, located sufficiently distant to approximate that all incident photons will be perpendicular to the lens surface and have a consistent wavelength, phase, and amplitude. Second, it is assumed that all energy is collected at the designed focal point and not higher order foci. Third, photon absorption in the lens material is neglected as it changes with photon energy. Were absorption included, the same profile could have a significantly different efficiency depending on

the photon energy being assumed. Ideally, these basic assumptions will yield a calculated lens efficiency that is only representative of the accuracy of the fabricated silicon profile.

To calculate the efficiency of each fabricated silicon profile, the sample is first measured with an optical profiler (Veeco, WYKO NT1100). The height data is imported into MATLAB, and a unit length virtual photon ($\vec{a}$) is sent "through" each point and propagated to the lens focus. The induced phase shift at each point on the lens (Φ_{Lens}) caused by the measured local thickness of the silicon lens (t_{measured}) is calculated by:

$$\Phi_{\text{Lens}} = 2\pi \times \left(\frac{t_{\text{measured}}}{t_{2\pi}} \right) \qquad (6)$$

where $t_{2\pi}$ is the thickness of silicon required to produce a phase shift of 2π for the photon energy of interest. The phase shift caused by the change in path length (Φ_{Geom}) from the radial point (r) to the focal point (f) is then calculated by

$$\Phi_{\text{Geom}} = 2\pi \times \left(\frac{\sqrt{r^2 + f^2}}{\lambda} \right), \qquad (7)$$

where λ is the photon wavelength in meters. The final phase of the arriving photon (Φ_{Final}) at the focal point is then the difference of the two above phase shifts,

$$\Phi_{\text{Final}} = \Phi_{\text{Geom}} - \Phi_{\text{Lens}}. \qquad (8)$$

Note that the difference of the phase shifts is calculated because the real part of the refractive index is slightly less than unity [12].

To account for the annular ring created by each measured point, assuming the measured profile is rotated through 360° to simulate a full lens, each
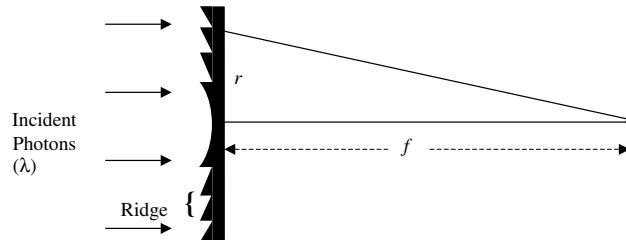

Fig. 3. Schematic used as the basis for developing a method to calculate the expected efficiency of a measured silicon profile.

phasor ($\vec{a}$) is scaled by its radial location (r) on the lens,

$$| \vec{a} | = 2\pi r \, dr, \tag{9}$$

where dr is determined by the horizontal measurement accuracy of the profiling system being used. The phase of each photon arriving at the focus (Φ_{Final}) is used to sum all incident phasors. Finally, the efficiency (η_{Lens}) is calculated by normalizing the resultant phasor by the sum of the magnitudes of each phasor sent 'through' the lens, and then squaring,

$$\eta_{\text{Lens}} = \left(\frac{| \sum\limits_{k=1}^{n} \vec{a}_k |}{\sum\limits_{k=1}^{n} | \vec{a}_k |} \right)^2. \tag{10}$$

Ideally, if each phasor has an identical Φ_{Final}, they will add perfectly (as if simply adding their magnitudes) and the lens efficiency will be 100%. It should be noted that this method is insensitive to any uniform vertical shifts, so an arbitrary datum may be used during the profile measurement.

To verify that the method described above is valid for calculating the lens efficiency for different profiles, we calculated the efficiency of a number of generated PFL profiles. Step approximation profiles using 2-steps, 4-steps, and 8-steps, as well as a smooth PFL profile, were generated based on (1). The efficiency of each profile was calculated using the method described above and compared to the efficiency theoretically predicted using [16],

$$\eta_{\text{Lens}} = \left[\frac{\sin (\pi/N)}{\pi/N} \right]^2. \tag{11}$$

The resulting calculated efficiencies of the generated profiles, shown in Table 1, are quite close to the theoretical values, within tenths of one percent. For the purposes of this research, Table 1 confirms that the method of approximating lens efficiency described in this section is sufficient to evaluate silicon PFL profiles fabricated using gray-scale technology.

5. Fabrication

All silicon wafers used in this research were 75 mm in diameter (due to equipment limitations), with a thickness of 450 μm. Lithography processing was performed using a GCA Ultratech wafer stepper system (5X reduction, $\lambda = 365$ nm). Clariant's AZ9245 positive photoresist was spun to a nominal thickness of 6μm, baked on a hotplate at 110 °C for 2 min, exposed 300 mJ, and hand developed in AZ400K (diluted 1:5 DI) for 8 min. No hard bake step was used. Further discussion on the gray-scale lithography process used for this research may be found in [9].

Etching was carried out in a Plasma-Therm 770 ICP DRIE system. The final DRIE recipe used an oxygen-only step that was added to the standard Bosch cycle to achieve the low etch selectivity necessary to fully transfer the gray-scale photoresist profile in such a shallow etch [11,14]. The final DRIE recipe is given in Table 2. The corresponding etch selectivity for this mask layout and etch recipe was 28:1. A total open area etch depth of 35.3 μm was achieved for the PFLs discussed later.

Table 1
Theoretical versus calculated lens efficiencies for various generated lens profiles

PFL profile	Lens efficiency	
	Theory	Calculated
2-Steps	40.5%	40.4%
4-Steps	81.1%	80.8%
8-Steps	95.0%	94.6%
Ideal	100.0%	99.6%

Table 2
DRIE recipe used to transfer gray-scale photoresist PFL pattern into the silicon

Step	Time (s)	Pressure (mTorr)	Power (W)	O_2 (sccm)	SF_6 (sccm)	C_4F_8 (sccm)	Ar (sccm)
Passivation	8	20	1	0	0	70	40
Etch	8	20	12	0	100	0	40
Oxygen-only	3	20	9	70	0	0	40

6. Results and discussion

6.1. Results

As explained earlier, since the annular ring defined by each PFL ridge will have the same collecting power, the efficiency of the outer ridges must be maximized for a particular design. In order to achieve the appropriate etch depth for the thin outer ridges in an uncompensated design, the wide central ridges on the sample will be over-etched due to the faster relative etch rate of larger features. Using the CARDE process, the wide central ridges are designed with a photoresist bias to mod-

ulate the time of etching to counteract the difference in etch rates, resulting in more controlled ridge heights and increased efficiency. Two devices, one uncompensated PFL and one CARDE PFL, fabricated simultaneously, are contrasted here to highlight this effect. For the CARDE PFL, the compensation function $(\delta(r))$ was constructed using $\delta_0 = 0.08$ and $R_{max} = 800$ μm. It should be noted that the lowest gray level (pixel) used in the optical mask design had an assumed normalized height in photoresist of 0.04. Since the lowest gray level is selected for the ridge bottom by default in both designs, the difference in design of the ridge bottom between the two PFLs was 0.04 (normalized) at the center and zero at the edge.

An SEM of a fabricated silicon PFL is shown in Fig. 4. Optical profiler scans were then taken of both the uncompensated and CARDE PFL profiles. Fig. 5(a) shows a scan of the uncompensated silicon profile, where the etch depth clearly changes as the radius increases and ridge width decreases. Conversely, Fig. 5(b) shows the CARDE silicon profile after etching where the etch depth has been controlled across the PFL despite the changing ridge width. Although the scans in Fig. 5 appear to show PFLs with truncated outer ridges, SEMs such as Fig. 4 prove otherwise. This apparent truncation is mostly an artifact of the low magnification used during the particular measurement and the thin, relatively high aspect ratio ridges at large radii. Higher magnification
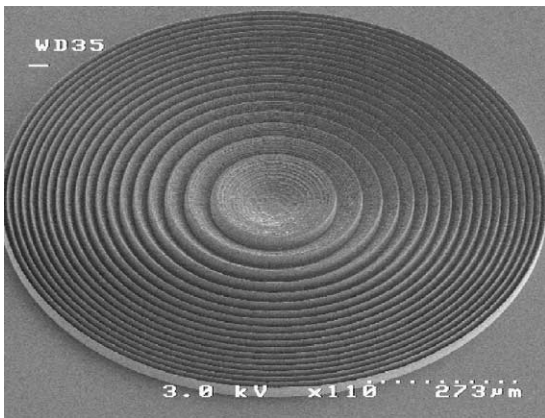

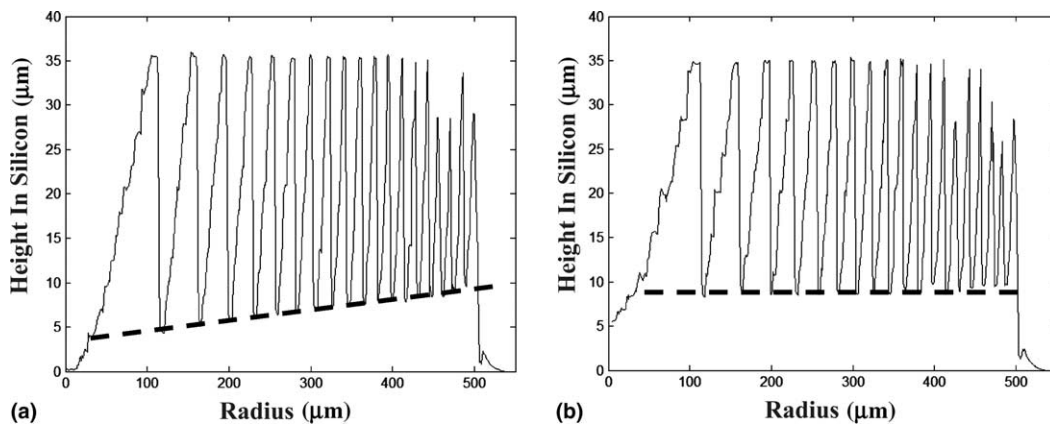Fig. 4. SEM image of a fabricated 1 mm diameter PFL containing 19 ridges.

Fig. 5. Measured silicon profiles for: (a) an uncompensated design, and (b) a CARDE design.

measurements capable of resolving ridge profile details were used to calculate profile efficiencies.

For the uncompensated PFL design shown in Fig. 5(a), the calculated efficiency of ridges at the edge of the profile ($r > 400$ μm) was 54%. Similarly, the CARDE PFL shown in Fig. 5(b) was found to have a calculated efficiency of 55% at the edge of the profile, an expected result since in both cases, the thin outer ridges had no compensation. These efficiencies also easily exceed the maximum theoretical efficiency of a binary Fresnel lens profile ($\sim$40%) that would be possible using planar fabrication techniques. Prospects for increasing this efficiency in the future will be discussed later.

Since the two PFLs have virtually identical edge efficiencies, it is reasonable to assume that the profile differences between the two PFL centers is a result of the introduced compensation function. Optical profiler scans were taken of the first four ridges ($r = 0 \rightarrow 250$ μm) and their efficiencies calculated. For the uncompensated profile, an efficiency of only 43% was calculated for the center of the PFL. Essentially, an extended etch time was used to improve the efficiency of the slow-etching outer ridges, which caused the fast-etching uncompensated central ridges to be over-etched. (Note the overall etch depth in Fig. 5 is greater than 35 μm, while a stepped profile should have a maximum height closer to 30 μm). In contrast, the CARDE PFL was measured to have a calculated efficiency of 80% for the same four central ridges. Since the different etch rates for each feature size were compensated by changing the etching time, the calculated efficiency for the CARDE PFL was almost twice as high as the uncompensated PFL. This large discrepancy in calculated efficiency clearly demonstrates the advantage of using the CARDE process to control the vertical dimensions of a 3D silicon profile despite changes in feature size that cause different etch rates across the pattern.

6.2. Discussion

To quantify the amount of 'traditional' ARDE during the same etch, rectangular trenches of various widths were included on the mask design, adjacent to the PFLs discussed above. Interest- ingly enough, the amount of lag was different for rectangular trenches and angled ridges of the same width. Fig. 6 shows a graph of etch depth versus trench/ridge width. From these measurements we see that rectangular trenches consistently etch deeper than angled ridges of the same width. We hypothesize that this small increase in ARDE seen in the angled ridges is due to the fact that the angled ridge has a consistent aspect ratio during the entire etch while the rectangular trench does not. For example, consider a wedge and rectangular trench on a single substrate, shown before etching in Fig. 7(a). As the etch proceeds, the horizontal and vertical dimensions of the silicon wedge both increase, effectively achieving and maintaining a single high aspect ratio throughout the etch, as shown in Fig. 7(b). In contrast, the full width of the rectangular trench begins etching immediately, so the initial aspect ratio of the trench is low, also in Fig. 7(b). Later during the etch, the rectangular trench etch depth increases while maintaining a constant width, which eventually increases its aspect ratio to that of the wedge, as shown in Fig. 7(c). Thus, for a given width, angled wedge structures will exhibit more ARDE since the ion/radical transport in/out of the trench is constrained during the entire etch, rather than only at the end.

Although we have shown here that PFLs created using gray-scale technology can exhibit high calculated efficiencies, it is useful to consider limi-
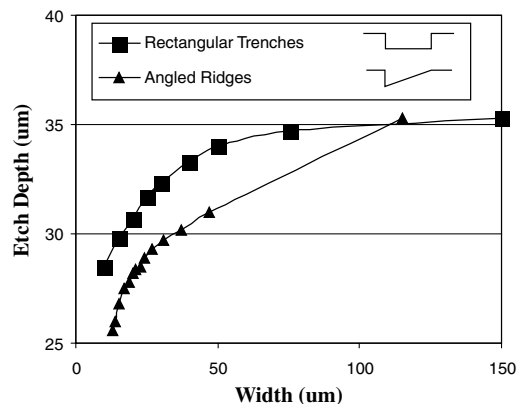

Fig. 6. Etch depth measurements for rectangular trenches and angled ridges of an uncompensated PFL.
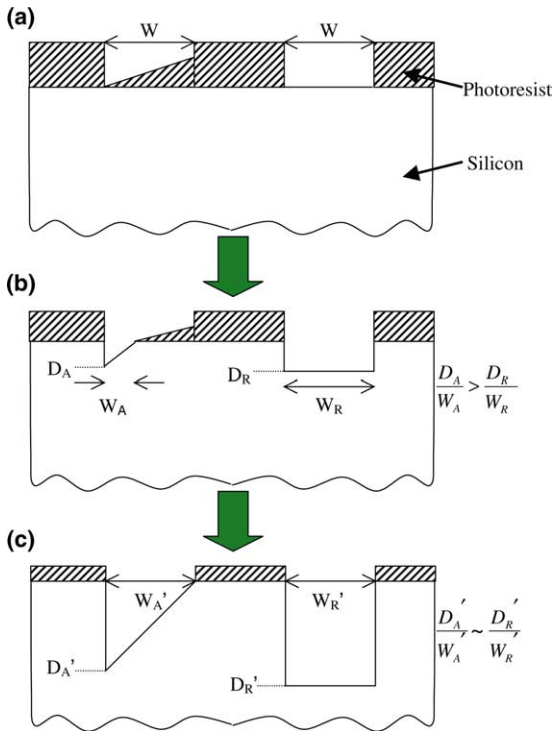
Fig. 7. Schematic of etch progression of angled and rectangular features. As the etch proceeds, the aspect ratio of the angled wedge remains high throughout, while the aspect ratio of the trench increases as the etch depth increases.

tations imposed by using this fabrication method and possible points of improvement:

First, the methods being used here, namely the Gaussian approximation and CARDE process, are empirical models for determining the optimum pixel layout for each structure. Thus, the profile accuracy will remain limited by the consistency with which the calibrated lithography process is repeated, and the accuracy of the Gaussian and CARDE approximations. Further development of these models will aide in the development of precise 3D silicon structures. However, in their current form these approximations have proven quite effective at accurately producing the desired profiles.

Second, the use of a pixilated design will limit the realistic minimum feature size in photoresist for 3D structures because multiple pixels are usually required to create a controlled 3D profile. Depending on the application, this limitation

may not be a problem, especially for MEMS applications where features >5 μm are required. This limitation is one reason that 4π phase depth designs were used in this research. By doubling the etch depth in silicon, each ridge width in photoresist was essentially doubled, allowing a larger number of pixels to be used to define a specific contour. The overriding tradeoff in using the increased phase depth design in our application is an increase in photon absorption due to the average PFL thickness doubling, which at high energies will become less significant.

Finally, the accuracy of the silicon PFL profiles was observed to be extremely sensitive to the pattern transfer during DRIE. Achieving the desired, low etch selectivity with the oxygen-only Bosch process discussed earlier was only moderately difficult, which we believe is a result of the timed oxygen-only step being the dominant factor in determining the etch selectivity. However, careful tuning of the passivation step is required because the passivation layer must prevent lateral etching of the photoresist during the oxygen-only step, without causing re-deposition or pinch-off during the etch step. This delicate balance typically results in a small 'flat' portion at the ridge bottom, approximately 3–4 μm wide for the ridges shown in Fig. 8. On wide ridges (>30 μm) a small 'flat' area has little effect on the overall profile accuracy and efficiency. However, as the ridges become smaller, the 'flat'
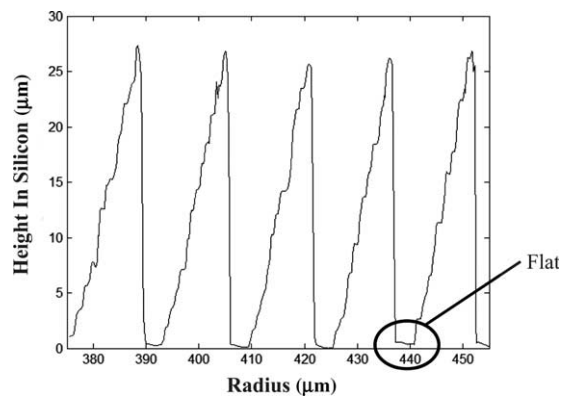

Fig. 8. Example outer PFL ridges on an uncompensated PFL design with a calculated efficiency of 57%. The small flat region at the ridge base arises from balancing of the passivation step during DRIE.

area becomes a significant portion of the entire ridge width and the overall accuracy of the profile is reduced, making high calculated efficiencies of thin outer ridges particularly challenging. For comparison, PFLs etched using a recipe with a shorter passivation step (6 s) caused a 5–6-μm 'flat', and resulted in calculated efficiencies below 25% for the thin outer ridges, despite appropriate etch depth and selectivity control.

We believe that through careful lithography process control, improved compensation functions, and further optimization of the DRIE pattern transfer, specifically further tuning of the passivation step, the efficiency of the outer PFL ridges on the current design can be increased. However, the PFLs presented herein provide an excellent demonstration of the advantages of using the CARDE process for further PFL development.

7. Conclusion

The gray-scale technology-based compensated aspect ratio dependent etching (CARDE) process was introduced to provide a vertical offset in photoresist to counteract the effects of aspect ratio dependent etching (ARDE) during deep reactive ion etching (DRIE). The CARDE process was demonstrated in the development of silicon X-ray phase Fresnel lenses (PFLs) to achieve controlled etch depths across a range of ridge widths. A phasor-based profile evaluation method confirmed that PFLs fabricated utilizing the CARDE process achieved a higher profile accuracy and calculated efficiency when compared to uncompensated lenses. Although used here to tailor the etch depths in a PFL, the CARDE process and design methodology presented in this paper can be easily integrated into a variety of 3D structure designs to achieve controlled silicon etch depths across a variety of feature sizes. Future work will include collaboration with NASA-Goddard Space Flight Center for the testing of these and other silicon PFLs in an X-ray beam line to evaluate their imaging performance.

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