Available online at www.sciencedirect.com
SCIENCE DIRECT®
Microelectronic Engineering 81 (2005) 106–116
MICROELECTRONIC ENGINEERING
www.elsevier.com/locate/mee

Substrate interconnect technologies for 3-D MEMS packaging

Brian Morgan [a,d], Xuefeng Hua [b,e], Tomohiro Iguchi [f], Taizo Tomioka [f], Gottlieb S. Oehrlein [c,e], Reza Ghodssi [a,d,*]

[a] Department of Electrical and Computer Engineering, A.V. Williams Building, University of Maryland, College Park, MD 20742, USA
[b] Department of Physics, University of Maryland, College Park, MD 20742, USA
[c] Department of Materials Science and Engineering, University of Maryland, College Park, MD 20742, USA
[d] Institute for Systems Research, University of Maryland, College Park, MD 20742, USA
[e] Institute for Research in Electronics and Applied Physics, University of Maryland, College Park, MD 20742, USA
[f] Toshiba Corporation, Corporate Manufacturing Engineering Center, Yokohama, 235-0017, Japan

Received 11 March 2005; received in revised form 11 April 2005; accepted 14 April 2005
Available online 3 May 2005

Abstract

We report the development of 3-dimensional silicon substrate interconnect technologies, specifically for reducing the package size of a MOSFET relay. The ability to interconnect multiple chips at different elevations on a single substrate can significantly improve device performance and size. We present the process development of through-hole interconnects fabricated using deep reactive ion etching (DRIE), with an emphasis on achieving positively tapered, smooth sidewalls to ease deposition of a seed layer for subsequent Cu electroplating. Gray-scale technology is integrated on the same substrate to provide smooth inclined surfaces between multiple vertical levels (>100 μm apart), enabling interconnection between the two levels via simple metal evaporation and lithography. The developments discussed for each technique may be used together or independently to address future packaging and integration needs.

Keywords: DRIE; Gray-scale lithography; 3-D substrate; Interconnects

1. Introduction

A metal-oxide-semiconductor field effect transistor (MOSFET) relay is switching device for small electrical signals commonly used for measurement equipment, making it an important component to the integrated circuit (IC) industry. Recently, there has been a demand for smaller packaging configurations of the MOSFET relay, as well as an improvement in high frequency signal passage. Therefore, we propose a new, smaller MOSFET relay package

* Corresponding author. Tel.: +1 301 405 8158; fax: +1 301 314 9281.
E-mail address: ghodssi@eng.umd.edu (R. Ghodssi).

0167-9317/$ - see front matter © 2005 Elsevier B.V. All rights reserved.
doi:10.1016/j.mee.2005.04.004

configuration based on a 3-dimensional (3-D) silicon substrate.

The outline of a conventional MOSFET relay package, shown in Fig. 1(a), contains three separate devices: a light emitting diode (LED), the MOSFET, and the Driver chip. Traditionally, the chips are connected by wire bonding and the package is shielded by plastic molding. Fig. 1(b) shows the proposed relay package, at approximately one-half the size of the conventional package. The combination of a 3-D silicon substrate (in place of the lead-frame) and flip-chip bonding to connect the MOSFET and Driver chip enables more dense packing of the components to reduce overall package size.

The 3-D substrate shown in Fig. 1(b) requires two primary interconnections methods to achieve the required performance. First, through-hole interconnects are required to establish connection between the MOSFET, the LED, and the bottom of the package. A number of groups have previously investigated the development of silicon vias for such vertical interconnects at a variety of dimensions with a variety of filler materials, such as polysilicon [1], solder [2], or copper [3–6]. For a MOSFET relay package, low-impedance interconnections are required, making copper the natural choice for filler material. However, since few connections are required, high-aspect ratio interconnects are unnecessary, leaving the primary challenges for this research as sidewall profile control and hole surface roughness (as high frequency signals will travel primarily on the surface of the metal).

The second interconnection technique is a tall, sloped silicon bulge that must be metallized to provide electrical connection between the base of the substrate and the second vertical level containing the Driver chip. Integrating through-holes and sloped bulges on a single 3-D substrate enables the use of simple surface metallization techniques on the top side to achieve vertical interconnects without the difficulty of plating vertical sidewalls or using complicated assembly techniques. Wiring of large, isotropically etched polymer surfaces has been demonstrated by Sharma et al. [7], however, isotropic etching in general is rather limited in the structures and geometries that can be achieved. An alternative technique, gray-scale technology [8–11] has the ability to make large, sloped structures in silicon using a single lithography step to form a variable height photoresist mask, which is subsequently transferred into silicon using plasma etching. Thus, gray-scale technology has been chosen for this research due to its flexible fabrication range and silicon's good mechanical and thermal properties as a substrate material.

In this paper, we introduce the design and process flow for a 3-D silicon substrate for the packaging of a MOSFET relay and its components. We then report the development of two fundamental interconnect technologies for creating 3-D substrates in silicon: through-hole deep reactive ion etching (DRIE) with positively tapered sidewalls, and sloped wiring using gray-scale technology. Although used here for a MOSFET relay, the techniques discussed in this paper can be used together or independently in the design and fabrication of future substrate technologies. Work regarding the assembly and testing of 3-D substrate-based MOSFET relays will be reported at a later date.

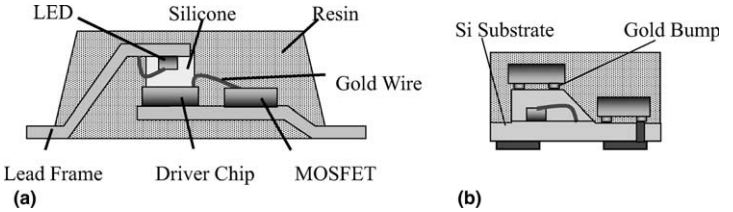

Fig. 1. Schematic cross-sections of (a) the conventional MOSFET relay package, and (b) the proposed MOSFET relay package utilizing a 3-D silicon substrate.

2. Substrate design

The basic design of the 3-D substrate is shown in Fig. 2. The substrate has three primary features. First, backside electrodes are connected to the substrate surface using large through-hole interconnects. Second, two large bulges are used to provide a vertical platform for attaching the Driver chip above the LED. And third, electrical connection between the top and bottom of the bulges is accomplished by patterning wires on a large, sloped surface on the side of the bulges.

Fig. 3 shows the process flow for creating such a 3-D substrate out of a single silicon wafer. First, the large bulge is created on the front side using gray-scale lithography and DRIE. Next, through-holes are etched from the backside, using a thermally grown oxide layer as an etch stop. Metal traces are then patterned on the topside, using spray-coating lithography, followed by electroplating to fill the etched through-holes (a second thermal oxide is grown for electrical isolation of the substrate). The final step is to attach the remaining three devices to the substrate, using flip-chip bonding for the MOSFET and Driver chip.

The success of creating this substrate is heavily dependent on two of these fabrications steps that will serve as the focus of the rest of this paper: the through-hole etching and the fabrication of a smooth bulge for sloped wiring.

First, both the sidewall profile and the surface roughness of the etched through-hole must be controlled precisely to ensure a uniform and continuous seed layer (techniques such as bottom-up plating using a handle wafer [4] are not realistic due to the integration with large top-side structures). If the through-hole becomes re-entrant (i.e., larger in diameter as the etch proceeds), sputtered metal seed layers will not coat the bottom of the trench well. Additionally, sidewall roughness must be minimized to avoid shadowing of the metal during deposition and to provide a smooth area for the passage of high frequency signals. Section 3 of this paper will outline the specific steps taken to tailor the sidewall profile of large vias during DRIE to ease seed layer deposition

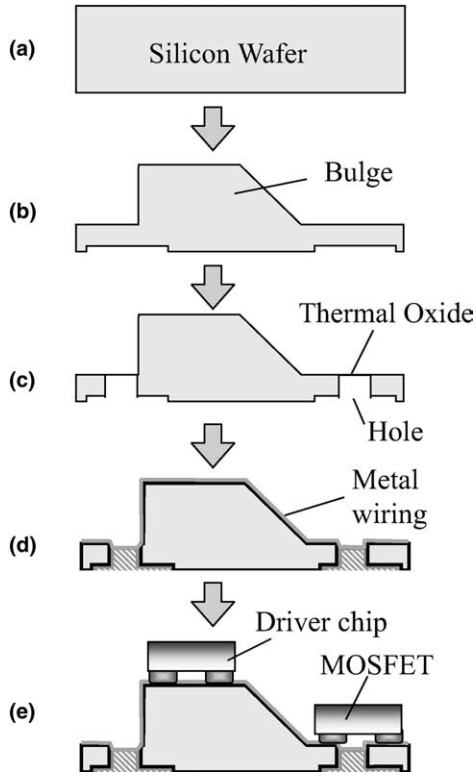

Fig. 3. Process flow for the MOSFET relay substrate. (a) Double polished silicon wafer. (b) Bulge is created using gray-scale technology. (c) Backside through-hole etch. (d) Metal deposition and patterning. (e) Flip-chip bonding of Driver chip and MOSFET.

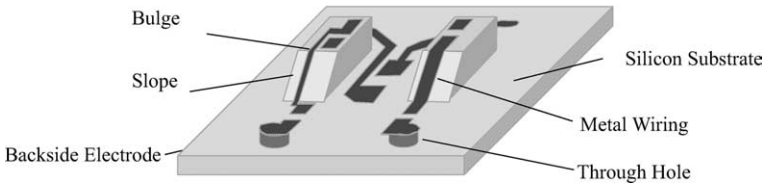

Fig. 2. Schematic of the MOSFET relay 3-D substrate incorporating two bulges with sloped wiring and through-hole interconnects.

for electroplating, as well as characterize the surface roughness of the deeply etched through-holes.

The second important fabrication challenge is to optimize the gray-scale technology process to achieve sloped wiring connections between multiple levels vertically separated by >100 μm. The primary concern for developing sloped interconnects is the surface morphology of the slope, since a single large step could prevent electrical continuity. The design, limitations, and experimental results for developing such an interconnect technique will be discussed in Section 4.

3. Through-hole etching

3.1. Design

A schematic of the through-holes developed in this work is shown in Fig. 4, where the top diameter is 150 μm and the depth is around 200 μm. The pattern was transferred using a 10 μm thick AZ9245 photo resist mask so that etch selectivity of the mask could be largely ignored. The aspect ratio is relatively low (<2:1) and the sidewall angle of this structure is typically re-entrant ($\theta > 90°$) due to its size and wide ion acceptance angle. However, in this work, we aim for positively tapered sidewall profiles, which is beneficial to the metal sputtering process for coating a film on the silicon sidewalls. A sidewall angle of 87° was desired, making the bottom diameter of the hole ≈130 μm. Additionally, considering the application of passing high frequency signals (that propagate near the metal surface), the sidewall roughness is specified to be <1 μm.

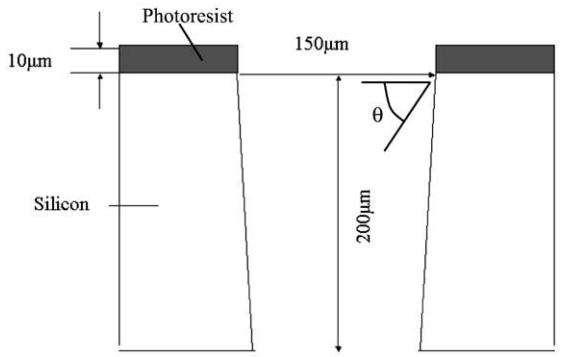

Fig. 4. Schematic of the desired silicon through-hole.

As mentioned earlier, DRIE using the Bosch process [12] will be used for deep silicon etching, in which etching and deposition cycles alternate in an ICP-RIE system to achieve a very directional deep silicon etch. The DRIE process typically uses an inductively coupled mode to produce a high-density plasma, which has good uniformity at low pressure. Capacitively coupled power is used to bias the substrate, allowing independent control of the ion energy. The DRIE reactor used for this work (STS Mesc Multiplex System) was used to process 100 mm diameter wafers.

3.2. Etch recipe development

The standard recipes recommended by the tool manufacturer are shown in Table 1. Silicon wafers coated with 10 μm AZ9245 photoresist mask were processed in DRIE for about 50 min using both the *high rate* and *low rate* recipes. Fig. 2 shows the SEM cross-section images (tilted 5°) for these two recipes. The etch depths are 94 and 184 μm for the *low* and *high rate* recipes, respectively, corresponding to etch rates of 1.89 and 3.69 μm/min. Both the lower bias power and lower chamber pressure contribute to the decrease in etch rate seen for the *low rate* case (see Fig. 5).

For low aspect ratio features, large ion acceptance angles and significant ion deflection from the mask often overwhelms the sidewall fluorocarbon layer (particularly for the *low rate* case causing striations). Thus, structures with low aspect ratios (in our case <2:1) exhibit predominantly re-entrant sidewall angles. In the figure, the diameter of the hole at the top is 150 μm in both cases, but the diameter at the bottom of the hole is 150 μm for *low rate* recipe and 158 μm for the *high rate* (sidewall angles of 90° and 92°, respectively). To achieve a positively tapered sidewall angle (<90°), the fluorocarbon passivation layer must survive long enough to prevent lateral etching and to promote slight growth towards the center. The survival of this fluorocarbon layer will depend on its thickness and etch rate, both of which can be controlled within the DRIE recipe. The use of

Table 1
Standard recipes from DRIE tool manufacturer

Recipe	Step	Pressure (mTorr)	Bias power (W)	RF power (W)	SF_6 (sccm)	C_4F_8 (sccm)	O_2 (sccm)	Step time (s)
High rate	Etch	30	17	600	130	0	13	10
	Passivation	30	0	600	0	85	0	6.5
Low rate	Etch	15	14	600	130	0	13	7
	Passivation	15	0	600	0	85	0	5

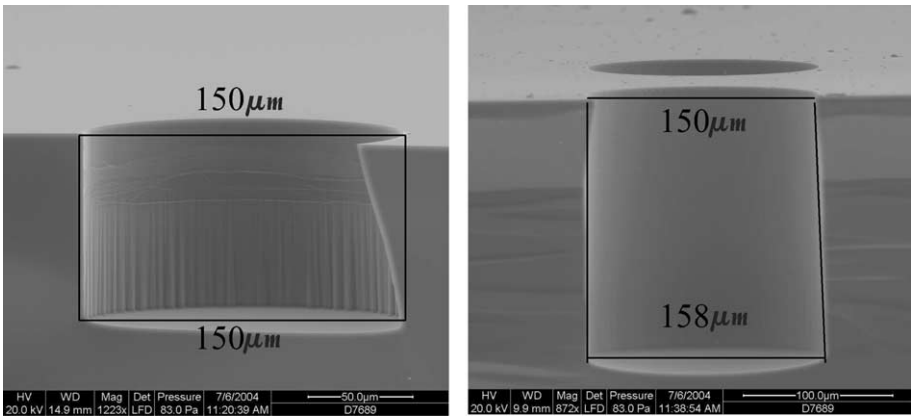

Fig. 5. SEM images of silicon holes etched using the low rate (left) and high rate (right) etch recipe.

lower bias powers should reduce the etch rate of this fluorocarbon layer, while longer passivation cycle times should increase the layer thickness.

The second major concern for our through-holes is sidewall roughness because of our eventual high frequency application. Fig. 6 shows enlarged SEM images of the sidewall for a through hole etched with (a) *low rate* recipe and (b) *high rate* recipe. While the peak–peak roughness scales are comparable for both recipes, the topography of the sidewall is strongly dependent on the process conditions. In both cases, the

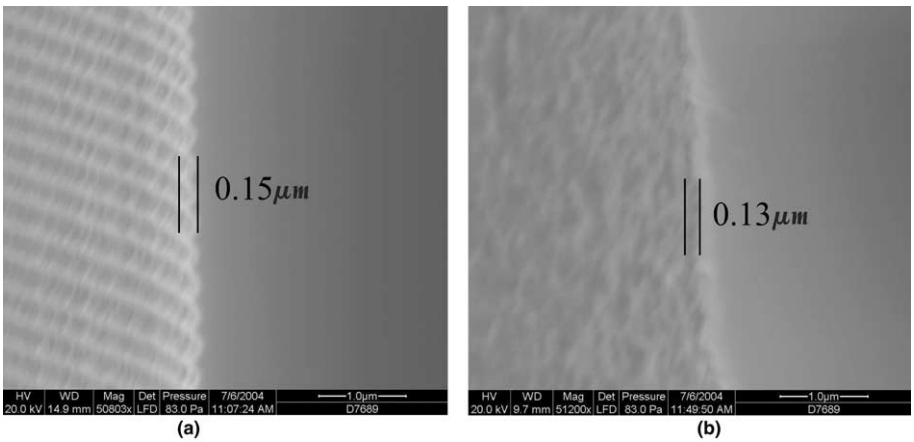

Fig. 6. SEM images of the sidewall roughness resulting from (a) low rate and (b) high rate etch recipes.

roughness is well below the 1 μm specification. Thermal oxidation and strip can reduce the roughness slightly (from 0.15 to ~0.09 μm for the *low rate* case), but is unnecessary given the initially low roughness.

Based on these initial results, further development of the through-hole interconnects is focused on the sidewall profile. Ayon et al. [13] have previously shown that positively tapered sidewall profiles could be formed rather easily for thin trenches (<20 μm), but as the trench width increased, the profile became more re-entrant. We chose to extend upon the work of Craigie et al. [14] who demonstrated that re-entrant sidewall angles of larger features could be controlled simply by tuning of the passivation step. In our case, to achieve positively tapered sidewalls on large vias (150 μm), it is necessary to drastically enhance the fluorocarbon passivation relative to etching, while avoiding excess fluorocarbon deposition that may cause micro-masking, grass formation, and/or irregular hole shapes.

There are many options to change fluorocarbon deposition/removal. One easy step is to remove the oxygen from the recipe, as oxygen plasma is well known as an efficient stripping discharge for polymers. Reduced bias power and increased passivation layers will also increase fluorocarbon removal time. Since the *low rate* recipe showed slightly higher roughness on the sidewall, as well as large striations, the high rate recipe was chosen as a starting point. The three parameters just mentioned were changed in succession while leaving other parameters constant. The results of initial modifications of the standard *high rate* recipe are summarized in Table 2.

All of the individual modifications provided some improvement of the sidewall profile, while the longer passivation cycle was the most effective. Combining all three modifications, i.e., 14 W bias power, no O_2, and 8-s passivation cycle, the sidewall angle was only improved to 89.5°. Longer passivation cycles were then examined and the results are shown in Fig. 7 for passivation cycles of

Table 2
Initial modifications to standard high rate recipe and resulting sidewall angle

	Bias power (W)	O_2 (sccm)	Passivation cycle time (s)	Sidewall angle (°)
Standard (high rate)	17	13	6.5	92
1	17	0	6.5	91
2	17	13	8	90
3	14	13	6.5	90.5

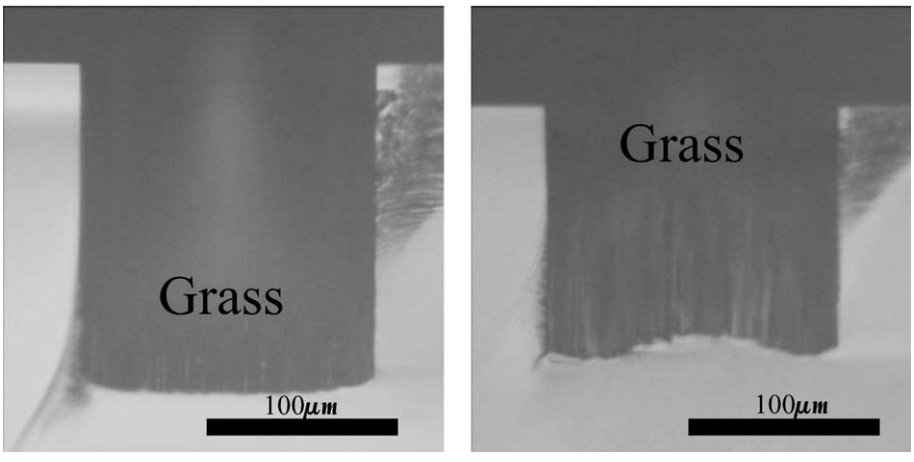

Fig. 7. Cross-sections of samples etched with 10 s (left) and 12 s (right) passivation cycle times.

(a) 10 s and (b) 12 s. The sidewall angles are 89° and 87.3° for the two cases, respectively. Unfortunately, a significant amount of grass was formed during each process because of excessive fluorocarbon passivation (much worse for the 12 s case). For the 10-s passivation case, the grass was triggered at the depth of about 120 μm and remained shorter than 50 μm in height. Since the etchant and neutral flux declines with increasing depth due to sidewall shadowing, and longer fluorocarbon passivation cycles require more etchant (fluorine) to be removed, it is likely that complete fluorocarbon removal becomes impossible at certain depth. The residual fluorocarbon material forms a micro mask for the silicon etching, which generates the grass.

The shapes of the hole bottom are also indicative of the fluorocarbon removal during the process. A comparison of neutral receiving angles of different positions at the hole bottom reveals a slight decrease in angle from the center to the side of the hole. Thus, during the etching cycle there is more material removal at the center, while during the passivation cycle more material grows at the center. If the fluorocarbon deposition is significant and the removal of the fluorocarbon is insufficient, the etch rate at the center is the lowest and the shape of the bottom exhibits a ripple at the center, as seen in Fig. 7, which is not observed in the conditions with sufficient etching time.

The above discussion suggests that the fluorocarbon deposition during the process is the key to control the through-hole profile. It is possible to achieve tapered sidewalls by using long passivation cycle or reducing the relative etching. But at the same time, the increase of fluorocarbon deposition is limited by other issues, e.g., grass formation, curved bottom shape. All these phenomena are caused by residual fluorocarbon during the etching cycle. If the residual time of fluorocarbon is short, the possibility of redepositing these species is low. Therefore, using low pressure during the etching cycle is a promising solution for eliminating grass formation. However, lower pressure will reduce the residual time of etchant species, causing an additional reduction of the etching rate.

Fig. 8 shows the results of etch rate and sidewall angles as a function of the passivation cycle time

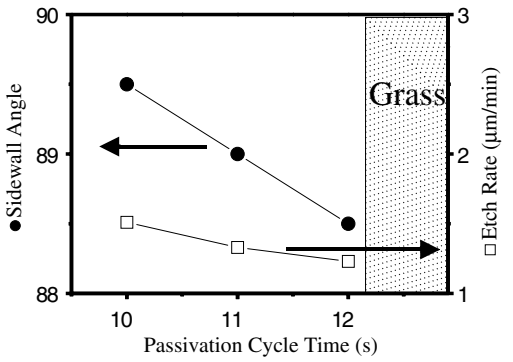

Fig. 8. Sidewall angle and etch rate as a function of passivation cycle time.

using a lower pressure during the etching cycle (15 mTorr). By lowering the pressure of etching cycle, grass formation was observed only for the passivation time greater than 12 s. The sidewall angle was improved to 88.5° with a final etch rate of 1.25 μm/min. The result is an etched through-hole with an initial diameter of 150 μm and a final diameter of ≈140 μm at the bottom. The resulting positively tapered sidewall profile will ease metal deposition of a seed layer for subsequent copper electroplating.

4. Sloped wiring using gray-scale technology

4.1. Design

The second interconnect technology being developed in this research is the formation of sloped wiring using gray-scale technology, which uses a single lithography step to form a variable height photoresist mask that is transferred into silicon using DRIE.

Gray-scale lithography may be performed in a number of ways [8,10,15,16]. The implementation used here relies on numerous sub-resolution opaque pixels with a fixed spacing, or pitch, as shown in Fig. 9. During subsequent projection lithography, the spatial information of each pixel is filtered out, and the intensity profile seen at the wafer corresponds to the size of the pixels used at each location.

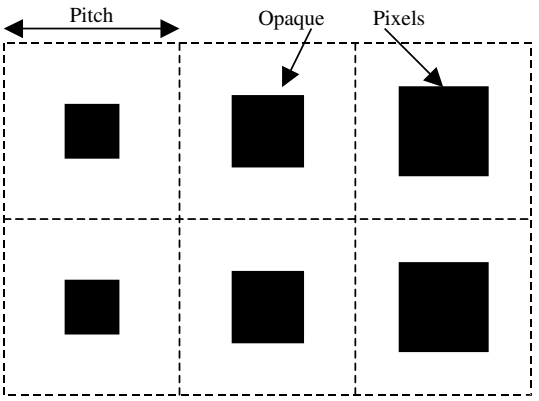

Fig. 9. Gray-scale optical masks use sub-resolution opaque pixels with a fixed spacing, or pitch [10].

Due to optical mask fabrication limitations, a limited number of different size pixels can be designed for a particular pitch. By using the minimum spot size (~100 nm) as an increment in pixel width or length, a pixel set containing >50 pixels was easily created for a pitch of 3 μm on the mask. The pixel layout method followed that of [11], where an optimized gray-scale lithography process is performed using a calibration mask, and a Gaussian curve is used to relate the pixel size and resulting height in photoresist.

Using a fixed increment in pixel *width* creates a change in pixel area proportional to its *length* ($\Delta\text{Area} = \text{Increment} \times \text{Length}$), and vice versa. Thus, the increment in pixel area between two small pixels creates small gray level steps in photoresist. Conversely, there will be a large increment in pixel area between two large pixels, creating larger gray level steps at the top of photoresist structures. The use of pitch values slightly above the resolution of the projection lithography system increases the number of pixel permutations, allowing smaller steps between gray-levels. Since a single gray level step of a few micrometers could prevent electrical connection down the tall (>100 μm) gray-scale slope, post-processing of the photoresist and silicon slopes has also been investigated.

4.2. Lithography

As discussed in [10], gray-scale lithography benefits from the use of thick, low contrast photoresist. Clariant's AZ9245 positive photoresist was selected for this work, spun to a nominal thickness of 10 μm. Exposure of the photoresist was performed using a 5X reduction projection lithography system (resolution ~0.5 μm) at the Cornell Nanofabrication Facility (www.cnf.cornell.edu). The relevant lithography process parameters are given in Table 3.

As mentioned previously, the gray-scale slope must be as smooth as possible, even though the number of gray levels will be limited. Thus, a hard-baking step was added to the gray-scale lithography process from [10] (following the development step) in an attempt to cause limited photoresist re-flow to improve the smoothness of the slope. Fig. 10 shows profilometer scans of two photoresist structures before and after the hard bake step.

In the case of the gray-scale slope, Fig. 10(a), the bottom of the slope is initially quite smooth, while the top of the slope contains gradually larger steps due to the constant pixel increment discussed earlier. After the hard bake step, the photoresist re-flow has significantly improved the smoothness of the entire profile. However, Fig. 10(b) shows a large planar structure before and after the hard bake, where the photoresist horizontal dimensions and sidewall profile have changed. The dimensional change of 15–20 μm for this large planar structure is acceptable for our application, as only

Table 3
Gray-scale lithography process parameters

Photoresist	Spin	Pre-bake	Exposure	Development	Hard-bake
Clariant AZ 9245	5 s at 300 rpm 40 s at 900 rpm → 10 μm	3 min at 110 °C (hotplate)	~800 mJ	AZ400k 1:4 DI 6 min	1 min at 110 °C

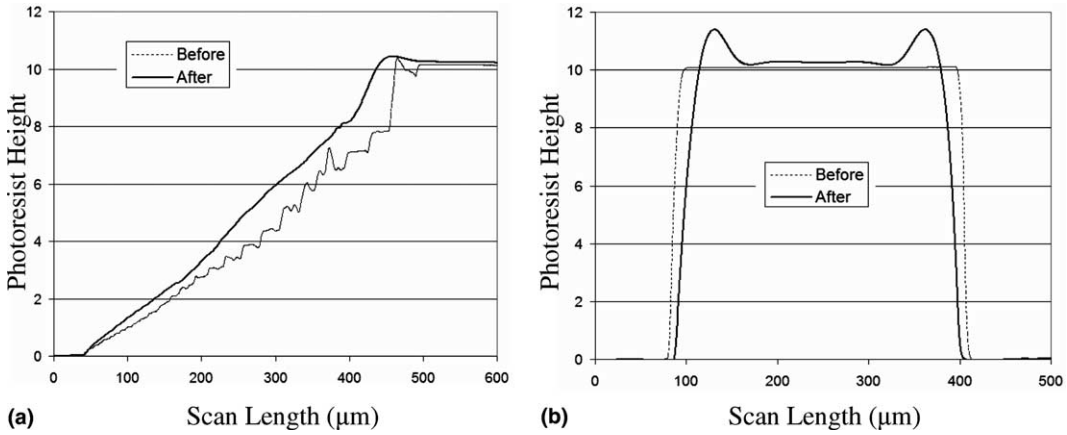

Fig. 10. Profilometer scans of (a) gray-scale photoresist slope and (b) planar structure, before and after a hard-bake step. The gray-scale slope becomes remarkably smoother, while the planar structure loses some dimensional accuracy.

large planar structures are defined during this step. However, for applications requiring strict planar dimension control, the photoresist re-flow method may be inappropriate or require further optimization (such as tailoring baking temperature and/or time). The change in photoresist sidewall profile (no longer vertical) may also result in rough silicon sidewalls due to slight mask erosion during the DRIE step.

4.3. Pattern transfer

The integration of gray-scale lithography with deep reactive ion etching (DRIE) has been demonstrated previously [9,11,17,18]. Contrary to the DRIE experiments for through-hole etching discussed earlier in this paper, the most important parameter for the transfer of the gray-scale structure into the silicon is the etch selectivity (the relative etch rates of silicon and photoresist), which defines the vertical amplification of the photoresist structure into the final silicon structure. To enable sloped wiring of various structure heights, a range of etch selectivity is required to amplify the photoresist slopes into different heights/angles. Previous investigations discuss wide tuning of etch selectivity during gray-scale pattern transfer, so only a brief discussion of the etch selectivity tuning is provided here [18]. It should be noted that the same silicon slope can be achieved using different combinations of slope height in photoresist and etch selectivity during DRIE.

Given the high silicon loading of the 3-D substrate pattern in this research, the initial selectivity achieved using the standard *high rate* recipe (given previously in Table 1) was quite low (<30). Some basic modifications to this recipe were made to increase the etch selectivity. First, O_2 was removed completely from the recipe, as O_2 discharges are known to etch photoresist very quickly. The bias power was also lowered from 17 W down to 10 W to reduce the ion bombardment sputtering of the photoresist during the etch cycle. In addition, a significant increase in etch selectivity was

Table 4
Etch selectivity tuning achieved by changing bias power and pressure

Recipe	Bias power (W)	Pressure (mTorr)	Etch rate (μm/min)	Etch selectivity
1	14	23	2.6	33
2	14	40	2.4	51
3	10	23	2.3	53
4	10	40	2.3	68

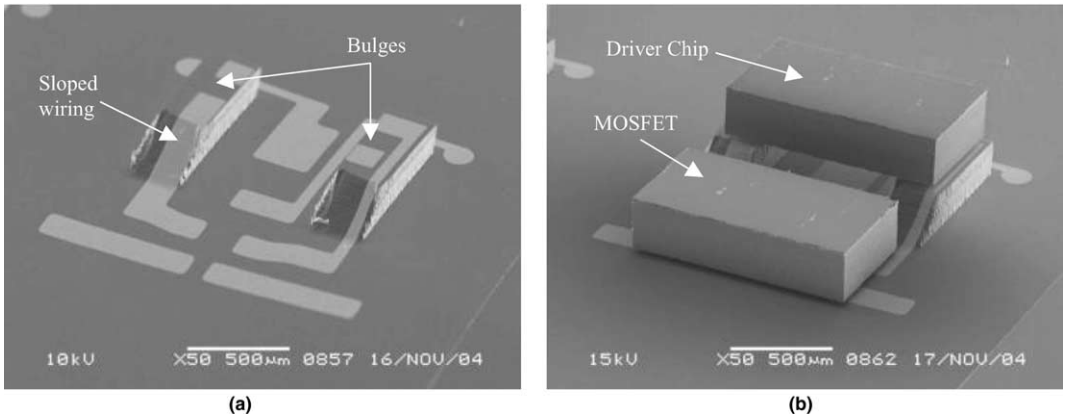

Fig. 11. (a) Silicon substrate with patterned metal traces providing electrical contact between the two levels. (b) Flip-chip bonding of multiple ICs illustrates the potential configuration for a MOSFET relay.

observed by increasing the pressure during the etch cycle. To avoid grass formation during the pattern transfer, short deposition cycles (~3 s) were used to minimize the amount of passivation layer to be removed. Table 4 shows four etch recipes and their corresponding etch selectivity. By establishing recipes with higher-than-necessary etch selectivity, parameter tuning for alternative etch properties may be performed. For example, using lower pressure will reduce etch selectivity but could improve wafer uniformity [13].

The average roughness on the gray-scale slopes immediately after DRIE was measured to be less than 50 nm. Simple post-processing steps, such as isotropic plasma etching and thermal oxidation, have been used to further improve the sloped surface morphology. Alternative methods, such as hydrogen annealing [19], could be used for dramatic smoothing of the silicon profile if desired.

4.4. Metallization

The final step in developing 3-D sloped interconnects is to define metal traces down the slope and verify electrical continuity. A Ti/Au (60/300 nm) layer was evaporated over the entire substrate. Since the substrate has already undergone DRIE, spin coating of photoresist is not feasible, so photoresist spray coating was performed at the Toshiba Corporate Manufacturing Engineering Center in Yokohama, Japan. Contact lithography was used to pattern this photoresist layer and wet etching removed the excess metal, leaving various metal traces on the 3-D substrate, as shown in Fig. 11(a). Electrical continuity was verified between the top of this 170 μm tall bulge and the bottom of the etched open area, confirming that the final gray-scale silicon slope was sufficiently smooth for even a thin (360 nm) metal layer. Fig. 11(b) shows example ICs after flip-chip bonding, demonstrating the ability to interconnect multiple ICs at different elevations on the same substrate.

The successful wiring of gray-scale sloped bulges >100 μm tall confirms that the sloped surface is indeed quite smooth. However, as the bulge height increases, as a result of higher etch selectivity, maintaining a smooth profile along the entire slope becomes increasingly difficult. Further post-processing of the slope and thicker evaporated metal layers are being investigated as methods of ensuring electrical contact down taller (~400 μm) slopes. Once electrical continuity is achieved, even if the connection is marginal, thick electroplating can be utilized to fill-in small gaps to provide a robust, low impedance interconnect between the two levels.

5. Conclusion

We have successfully demonstrated two interconnect technologies for creating next generation

3-D silicon substrates. Through-hole interconnects were optimized by tailoring the etch power and passivation cycle time during DRIE to control sidewall profile and morphology, easing deposition of a thin metal seed layer for subsequent copper electroplating. Gray-scale technology was then used to demonstrate a sloped wiring technique capable of providing interconnection between multiple vertical levels on a single silicon substrate. These two technologies can be used individually or in tandem to address a multitude of substrate and packaging issues, including the small MOSFET relay configuration proposed here.

Acknowledgments

This paper is the result of joint research between UMD and Toshiba Corporation. The structures discussed in this work were fabricated and characterized using the cleanroom at the Institute for Research in Electronics and Applied Physics (IREAP) and the MEMS Sensors and Actuators Lab (MSAL) at University of Maryland. Projection lithography exposures were carried out at the Cornell Nanofabrication Facility in Ithaca, NY. Pattern wiring and assembly processes were carried out at the Toshiba Corporation. Brian Morgan is the recipient of the Achievement Rewards for College Scientists (ARCS) Fellowship (Metropolitan Washington Chapter) for 2004–2005 and 2005–2006.

References

[1] E.M. Chow, V. Chandrasekaran, A. Partridge, T. Nishida, M. Sheplak, C.F. Quate, T.W. Kenny, J. Microelectromech. Syst. 11 (6) (2002) 631–640.
[2] R.A. Lee, W.A. Moreno, R.A. Gassman, D. Miller, in: Proceedings of 1992 13th IEEE/CHMT International Electronic Manufacturing Symposium, Baltimore, MD, 28–30 September, 1992.
[3] M.A.S. Jaafar, D.D. Denton, J. Electrochem. Soc. 144 (7) (1997) 2490–2495.
[4] N.T. Nguyen, E. Boellaard, N.P. Pham, V.G. Kutchoukov, G. Cracium, P.M. Sarro, J. Micromech. Microeng. 12 (2002) 395–399.
[5] S. Spiesshoefer, L. Schaper, S. Burkett, G. Vangara, Z. Rahman, P. Arunasalam, in: 2004 Electronic Components and Technology Conference, 2004, pp. 466–471.
[6] S.L. Burkett, X. Qiao, D. Temple, B. Stoner, G. McGuire, J. Vac. Sci. Technol. B 22 (1) (2004) 248–256.
[7] V. Sharma, A.B. Suriadi, F. Berauer, L.S. Mittelstadt, in: Materials, Technology and Reliability for advanced Interconnects and Low-k Dielectrics Symposium, San Francisco, CA, 21–25 April, 2003.
[8] Gal, US Patent 5 310 263, 1994.
[9] M.R. Whitley, R.L. Clark, J.R. Shaw, D.R. Brown, P.S. Erbach, G.T. Dorek 2002 International patent WO 02/31600 A1.
[10] C.M. Waits, A. Modafe, R. Ghodssi, J. Micromech. Microeng. 13 (2003) 170–177.
[11] B. Morgan, C.M. Waits, J. Krizmanic, R. Ghodssi, J. Microelectromech. Syst. 13 (2004) 113–120.
[12] F. Laemer, A. Schilp, Robert Bosch GmbH, US patent 5(501), 1996, p. 893.
[13] A. Ayon, R. Braff, C. Lin, H. Sawin, M.A. Schmidt, J. Electrochem. Soc. 146 (1) (1999) 339–349.
[14] C.J.D. Craigie, T. Sheehan, V.N. Johnson, S.L. Burkett, J. Vac. Sci. Technol. B 20 (6) (2002) 2229–2232.
[15] W. Henke, W. Hoppe, H.J. Quenzer, P. Staudt-Fischbach, B. Wagner, in: Proceedings of the IEEE International Conference on Micro Electro Mechanical Systems (MEMS 1994), 1994, pp. 205–210.
[16] Canyon Materials, Inc., US Patent 5,285,517, 1994.
[17] B. Morgan, C.M. Waits, R. Ghodssi, Microelec. Eng. 77 (1) (2005) 85–94.
[18] C.M. Waits, B. Morgan, M.J. Kastantin, R. Ghodssi, Sensor Actuat. A: Phys. 119 (2005) 245–253.
[19] M-C.M. Lee, M.C. Wu, in: Proceedings of the 2004 Solid-state Sensor, Actuator and Microsystems Workshop, Hilton Head Island, South Carolina, June 6–10, 2004, pp. 19–22.